Forming Virtual Traces for WCET Analysis and Reduction

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Propose CPU modifications for:

1. accurate *worst case execution time* (WCET) analysis.

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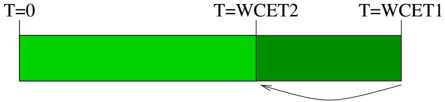
2. improved *guaranteed throughput* (versus a simple CPU).



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- restrict this operation so that:
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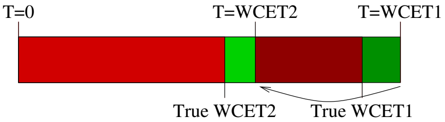
  - the WCET analysis model won't include any *pessimistic* assumptions.



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How do traces meet the requirements?

Previous work

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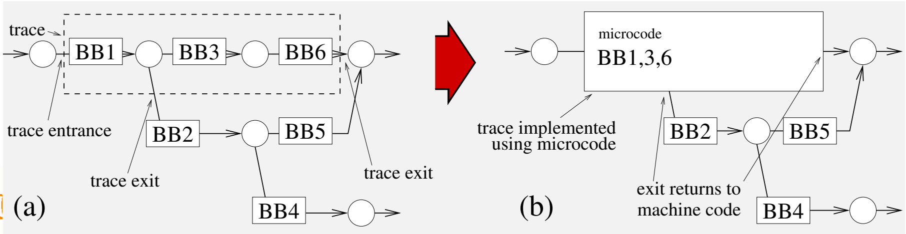
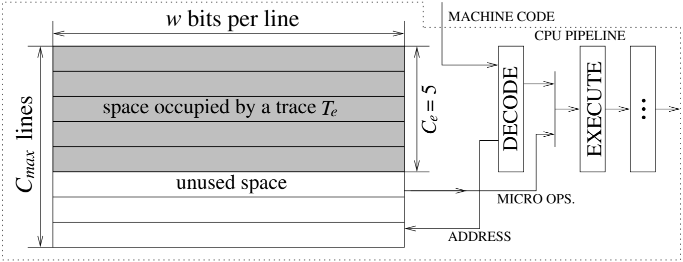


Previous work

4. Allocate space in a *trace scratchpad* for microcode.
   The microcode is used in place of the original machine code.



J. Whitham and N. Audsley, Using trace scratchpads to reduce execution times in predictable real-time architectures, Proc. RTAS, 305–316, 2008.

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- the poor code density of microcode.

Result: No microcode. The virtual trace controls a conventional *but constrained* dynamic CPU scheduler.

Implementation

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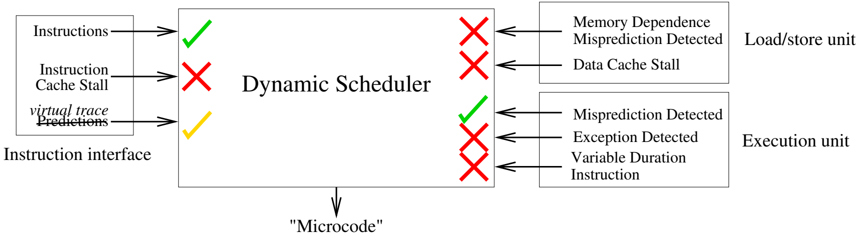
2. Handle all events that could change execution times.



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- The CPU is its own timing model.

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- **Now**: space limit is less restrictive, so the whole program should be translated.
- This problem is similar to selecting static branch predictions to minimize WCET.

F. Bodin and I. Puaut. A WCET-oriented static branch prediction scheme for real time systems. In Proc. ECRTS, pages 33–40, 2005.

Proposed solution

Combine two algorithms:

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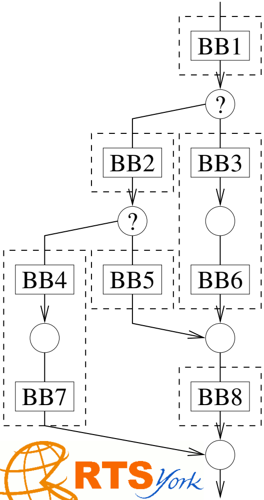
- Trace formation algorithm from previous work.
  - Form traces by following branch predictions.

Example



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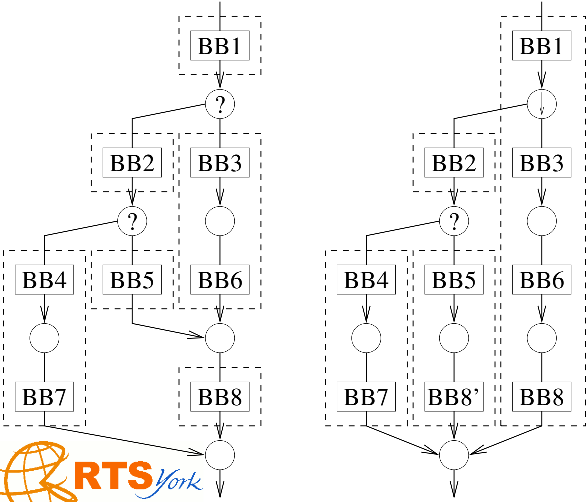
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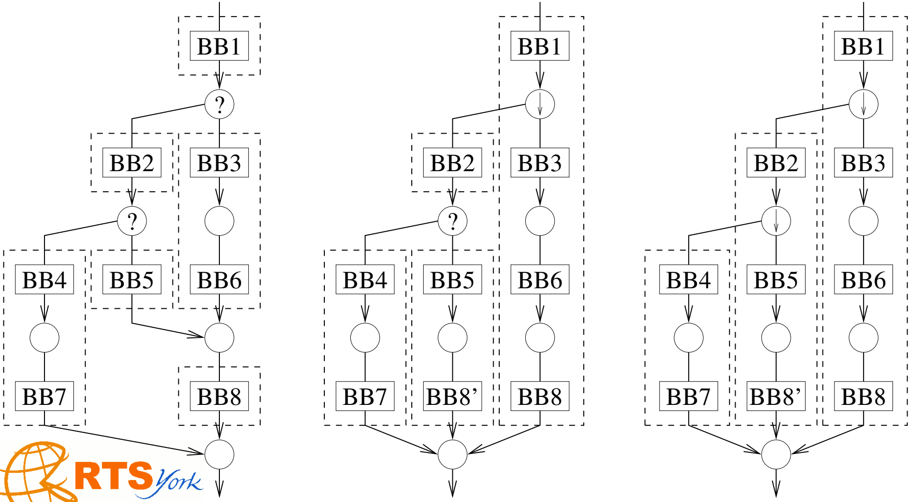

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Variable

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- Defined by the size of the memory for virtual traces.
- $L = 1 \Rightarrow$ Trivial traces: like assuming all branches are *unknown*.
- $L > 1 \Rightarrow$ Non-trivial traces: speculation is used to reduce the cost of the predicted execution path.

Experiment 1

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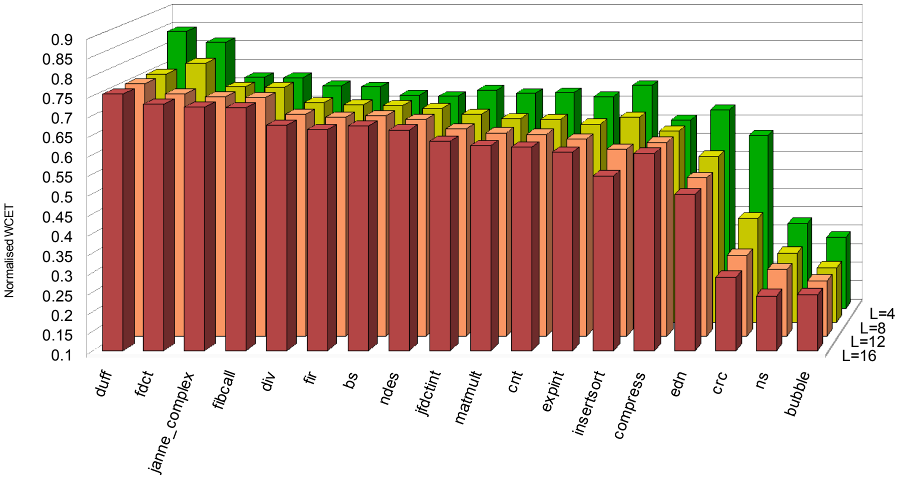
- Compare $L = 1$ against $L \in [4, 8, 12, 16]$ for various benchmark programs.
- Using experimental platform from:

J. Whitham. Real-time processor architectures for worst case execution time reduction. PhD Thesis YCST-2008-01, University of York, 2008.

Results 1

Normalized against results for $L = 1$.



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2. If an improvement is found, repeat step 1.

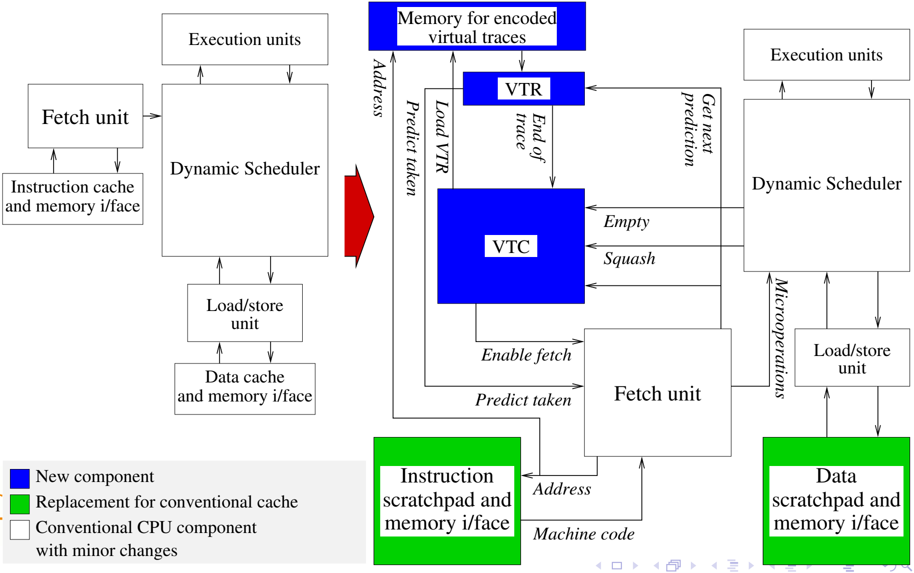
Results 2

Program	$L = 4$			$L = 16$		
	i	NW	%ch	i	NW	%ch
cnt	1	0.679	0.1%	1	0.618	0.1%
compress	3	0.604	0.2%	2	0.601	0.2%
edn	2	0.629	0.5%		n/a	
expint	1	0.668	0.0%	1	0.605	0.0%
fibcall	1	0.616	16.8%	1	0.616	16.8%
janne_complex	2	0.675	6.7%	2	0.675	6.7%
matmult	2	0.677	0.1%	2	0.622	0.1%
ndes	4	0.669	0.1%	5	0.661	0.2%
ns	3	0.305	7.9%	2	0.198	21.3%

Related Work

- Scratchpads
  Puaut, Suhendra, Wehmeyer
- Single-path paradigm
  Puschner
- Hybrid timing analysis
  Mohan, Mueller
- Dataflow-like computing models
  Lee et al.

Implementation



- New component
- Replacement for conventional cache
- Conventional CPU component with minor changes

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- Consequently, greater WCET reductions are possible.
- The greatest benefits of traces are seen when one execution path is much more costly than the others.
- Limiting virtual trace sizes to $L = 8$ is sufficient in many cases.
- The Bodin-Puaut algorithm is not optimal but only minor improvements are possible.

End

- All questions and comments are welcome!
- Further information:
  `http://www.jwhitham.org.uk/pubs/`